REMARKS

The June 28, 2006 Office Action was based on pending Claims 1–40. By this Response, Applicant is amending Claims 1, 14, 15, 22 and 24 and is cancelling Claims 13 and 23 without prejudice or disclaimer. Claims 2–12, 16–21 and 25–40 remain as originally filed.

Thus, after entry of the foregoing amendments, Claims 1–12, 14–22 and 24–40 are pending and presented for further consideration. In view of the foregoing amendments and the remarks set forth below, Applicant respectfully submits that Claims 1–12, 14–22 and 24–40 are in condition for allowance.

SUMMARY OF REJECTIONS

The June 28, 2006 Office Action rejected Claims 1, 9, 14, 15, 24 and 32 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,134,698 to Imamura et al. ("Imamura et al").

Claims 7, 8, 10–13, 20, 21 and 38–40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Imamura. Claims 2–6, 16–19, 22, 25–31 and 33–37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Imamura in view of U.S. Patent No. 5,548,730 to Young et al. ("Young"). Claim 23 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Imamura in view of U.S. Patent No. 5,222,225 to Groves ("Groves").

CLAIM REJECTIONS UNDER 35 U.S.C. § 102(b)

The Office Action rejected Claims 1, 9, 14, 15, 24 and 32 as being anticipated by Imamura. In view of the foregoing amendments and for at least the reasons set forth below, Applicant respectfully disagrees and requests reconsideration of Claims 1, 9, 14, 15, 24 and 32.

Independent Claim 1

Focusing on amended independent Claim 1, in one embodiment of Applicant's invention a method is disclosed for performing data string operations. The method comprises (i) routing a series of instructions to a general purpose microprocessor having a first execution unit for executing instructions and (ii) analyzing the instructions

to detect an instruction to perform a data string operation. An undecoded version of the data string operation instruction is then routed to a second execution unit. The method further includes controlling read and write operations to and from external memory via control circuitry with each of the first execution unit and the second execution unit without intervention by the other execution unit.

Imamura does not disclose the method recited by independent Claim 1. Rather, Imamura concerns a data processing system having an instruction processor, a storage controller and storage (see Abstract). As described with reference to Figure 1, the system of Imamura transfers data between a main storage 4 and an extended storage 5. In doing so, the instruction processor 1 sends a transfer instruction to the storage controller 2 to complete the transfer of data (see, e.g., col. 5, lines 11–30).

Thus, the system of Imamura discloses a single component (i.e., the storage controller 2) for performing data transfer between the main storage 4 and the extended storage 5. Imamura does not disclose a method that utilizes two execution units to independently control read and write operations to and from an external memory. For instance, Imamura's instruction processor 1, which the Office Action labels a "general purpose microprocessor having a first execution unit," does not appear to control read and write operations to storage 4, 5 without intervention by the storage controller 2, which the Office Action labels a "second execution unit." Rather, the instruction processor 1 of Imamura must utilize the storage controller 2 to operate on the data in storage 4, 5.

Moreover, and alternatively, the system of Imamura does not appear to have a second execution unit that receives an undecoded version of a data string operation instruction that was also received by a general microprocessor having a first execution unit. Although Imamura discloses that its instruction processor 1 sends a transfer instruction to the storage controller 2, Imamura does not disclose that the transfer instruction is an undecoded version of the same instruction received by the instruction processor 1.

Because the cited art does not disclose a method that (i) utilizes two execution units, each capable of controlling read and write operations to the same memory

without intervention by the other and (ii) routes to a second execution unit an undecoded version of a data string operation instruction that was also received by a general microprocessor having a first execution unit, Applicant asserts that Claim 1 is not anticipated by Imamura. Applicant, therefore, respectfully requests allowance of Claim 1.

Independent Claims 9, 14, 15, 24 and 32

Independent Claim 9 is believed to be patentably distinguished over the cited art for reasons similar to those set forth above with respect to the patentability of amended independent Claim 1 and for the different aspects recited therein. For example, Imamura does not appear to disclose a processing system having "memory circuitry . . . configured to be alternatively controlled by [a] first execution unit and [a] second execution unit using the same memory control circuitry, wherein said first [and] second execution unit[s] are separately coupled to said memory control circuitry."

Amended independent Claim 14 is believed to be patentably distinguished over the cited art for reasons similar to those set forth above with respect to the patentability of amended independent Claim 1 and for the different aspects recited therein. For example, Imamura does not appear to disclose a processing system having "memory circuitry . . . configured to be alternatively controlled by [a] first execution unit and [a] second execution unit . . ., wherein said first execution unit is configured to operate said memory circuitry independently of said second execution unit, and wherein said second execution unit is configured to operate said memory circuitry independently of said first execution unit."

Amended independent Claim 15 is believed to be patentably distinguished over the cited art for reasons similar to those set forth above with respect to the patentability of amended independent Claim 1 and for the different aspects recited therein. For example, Imamura does not appear to disclose a method comprising "controlling read and write operations to and from memory . . . with [a] first execution unit via control circuitry and independent of [a] second execution unit" and "controlling read and write operations to and from said memory with said second execution unit via said control circuitry and independent of said first execution unit."

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Amended independent Claim 24 is believed to be patentably distinguished over the cited art for reasons similar to those set forth above with respect to the patentability of amended independent Claim 1 and for the different aspects recited therein.

Independent Claim 32 is believed to be patentably distinguished over the cited art for reasons similar to those set forth above with respect to the patentability of amended independent Claim 1 and for the different aspects recited therein. For example, Imamura does not appear to disclose a method including "routing a series of instructions to a general purpose microprocessor having a first execution unit; analyzing said series of instructions so as to detect an instruction to perform a data string operation; and routing said instruction to perform a data string operation to a second execution unit such that said first execution unit does not receive said instruction."

CLAIM REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 7, 8, 10–12, 20, 21 and 38–40 were rejected as being unpatentable over Imamura. Claims 2–6, 16–19, 22, 25–31 and 33–37 were rejected as being unpatentable over Imamura in view of Young.

In view of the foregoing amendments and for at least the reasons set forth below, Applicant respectfully disagrees and requests reconsideration of the aforementioned claims.

Independent Claim 22

Amended independent Claim 22 is believed to be patentably distinguished over the cited art for reasons similar to those set forth above with respect to the patentability of amended independent Claim 1 and for the different aspects recited therein. For example, neither Imamura, nor Young, nor a combination thereof, teaches of suggests a processing system having "dedicated string execution circuitry integral to said memory controller . . . and configured to perform string manipulation instructions on data in [a] memory integrated circuit without intervention by [a] host processing integrated circuit, and wherein said host processing circuit is configured to operate said memory controller independently of said string execution circuitry."

Dependent Claims

Claims 2–6 depend from amended independent Claim 1 and are believed to be patentably distinguished over the cited art for the reasons set forth above with respect to Claim 1 and for the additional features recited therein.

Claims 7 and 8 depend from amended independent Claim 1 and are believed to be patentably distinguished over the cited art for the reasons set forth above with respect to Claim 1 and for the additional features recited therein.

Claims 10–12 depend from independent Claim 9 and are believed to be patentably distinguished over the cited art for the reasons set forth above with respect to Claim 9 and for the additional features recited therein.

Claims 16–19 depend from independent Claim 15 and are believed to be patentably distinguished over the cited art for the reasons set forth above with respect to Claim 15 and for the additional features recited therein.

Claims 20 and 21 depend from independent Claim 15 and are believed to be patentably distinguished over the cited art for the reasons set forth above with respect to Claim 15 and for the additional features recited therein.

Claims 25–31 depend from independent Claim 24 and are believed to be patentably distinguished over the cited art for the reasons set forth above with respect to Claim 15 and for the additional features recited therein.

Claims 33–37 depend from independent Claim 32 and are believed to be patentably distinguished over the cited art for the reasons set forth above with respect to Claim 32 and for the additional features recited therein.

Claims 38–40 depend from independent Claim 32 and are believed to be patentably distinguished over the cited art for the reasons set forth above with respect to Claim 32 and for the additional features recited therein.

REQUEST FOR TELEPHONE INTERVIEW

Pursuant to M.P.E.P. § 713.01, in order to expedite prosecution of this application, Applicant's undersigned attorney of record hereby formally requests a telephone interview with the Examiner as soon as the Examiner has considered the

effect of the arguments presented above. Applicant's attorney can be reached at the general office number listed below.

CONCLUSION

In view of the foregoing, the present application is believed to be in condition for allowance, and such allowance is respectfully requested. If further issues remain, the Examiner is cordially invited to contact the undersigned such that the issues may be promptly resolved.
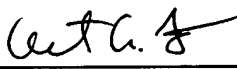
Moreover, by the foregoing amendments and remarks no admission is made that any of the above-cited references are properly combinable. Rather, Applicant submits that even if the references are combined, the references still do not teach or suggest the claimed invention.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: ___9/26/2006___   By: ___[signature]___

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